ICCAD 99

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THE INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS, INC.

AREAS OF INTEREST

Original technical papers on (but not limited to) the following topics are invited:

1) SYNTHESIS

1.1 Combinational logic optimization (area, timing, power). FPGA optimization. Don't care methods. Technology mapping.

1.2 Sequential synthesis and optimization (e.g., state encoding, retiming) for area, timing and power. Asynchronous circuit design.

1.3 High level synthesis (scheduling, allocation, and binding). Datapath, control and memory system synthesis and optimization. Estimation, use of libraries and synthesis environments.

1.4 Analog circuit synthesis, optimization and layout.

2) MODELING, SIMULATION, VERIFICATION AND TESTING

2.1 Circuit and interconnect-level simulation. Digital, Analog and RF circuit simulation techniques, circuit-level timing and power simulation. Interconnect parameter extraction and circuit model generation. Noise and crosstalk analysis, timing models for interconnect.

2.2 Timing Analysis. Circuit-level delay and False path analysis. Transparent latch timing analysis and clock schedule optimization.

2.3 Switch, logic and high-level modeling and simulation. Functional Design Verification. Formal verification techniques. High-level Design Validation.

2.4 Testing. New strategies for digital circuits and analog circuits. Fault simulation. Testability for digital circuits and analog circuits. BIST & DFT schemes. Partial and boundary scan.

2.5 Manufacturability Analysis. Yield estimation and statistical performance analysis.

2.6 Mixed Technology Simulation. Methods for mixed RF-analog-digital circuits, coupled packaging-circuit electrical and thermal analysis, coupled circuit-micromechanical simulation.

3) PLANNING, PLACEMENT AND ROUTING

3.1 Placement and floorplanning techniques (esp. high performance, large scale integrated systems). RTL Area estimation. Partitioning for layout. Module generation and layout synthesis.

3.2 Timing-driven/noise-avoidance routing. Automatic special net routing layout for manufacturability.

3.3 Complete layout systems. Layout migration. Symbolic design and compaction. Physical design planning. DRC, ERC, and layout verification. Interaction between logic synthesis and layout.

4) SYSTEM DESIGN AND PRODUCT ENGINEERING

4.1 Specification, modeling and design of embedded systems. Hardware/software co-design. Software synthesis, analysis and verification. Hardware/software co-testing and co-validation.

4.2 Interface synthesis. System integration and testability. Performance evaluation. Issues for real-time systems and DSP. ASIP synthesis.

4.3 Design metrics, concurrent engineering, requirements management, robust engineering, design for manufacturing, iterative methodologies, and planning and management. Design reuse and intellectual properties. Frameworks and CAD on internet. Middleware: intertool communication, databases and data management. Hardware design languages and user interface.

AUTHOR INFORMATION AND FORMAT

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  - Abstract, typed on separate page should state clearly and precisely what is new and point out the significant results. The IMPACT, or potential impact, of the contribution will play a major role in the evaluation.
- 1 paper of no more than 4 pages using proceedings format
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Papers in the wrong format or exceeding the restrictions described on the ICCAD Web page will automatically rejected.

- Previously published papers will not be considered; this includes Workshop Proceedings.
- For further information email: iccpubpap@dac.com
- Authors should clearly address the significance of their contribution as part of the paper.
- Proposals for Panel Sessions and Tutorials are also invited.

AUTHOR'S SCHEDULE

Deadline for submissions:	**April 9, 1999**
Notification of acceptance:	**July 12, 1999**
Deadline for final version:	**August 13, 1999**

Papers will not be accepted for submission after April 9, This deadline is firm and inflexible. No exceptions will be n

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